WHAT IS CLAIMED IS:

1. A method for fabricating a DRAM cell arrangement with vertical MOS transistors, comprising:

forming a source/drain material on a substrate;

etching trenches to form a plurality of parallel ribs having strips of the source/drain material disposed thereon, wherein the strips provide sites for a plurality of upper source/drain regions of the vertical MOS transistors;

depositing a covering layer on a floor of the trenches;

depositing a gate dielectric layer on the surfaces of the ribs;

filling the trenches, whereby gate electrodes for the vertical MOS transistors are produced on either side of the ribs;

forming a plurality of word lines over, and cross-wise with respect to, the ribs;

depositing a first auxiliary layer, capable of wafer bonding, on the plurality of word lines;

attaching a first auxiliary carrier substrate to the first auxiliary layer;

removing at least the substrate;

forming a plurality of lower source/drain regions on the ribs, wherein portions of the ribs disposed between the plurality of lower source/drain regions and the plurality of upper source/drain regions define channel regions for the vertical MOS transistors; and

forming shallow isolation trenches to isolate the plurality of lower source/drain regions.

2. The method of claim 1, further comprising forming capacitors stacked, with respect to the vertical MOS transistors, on the first auxiliary carrier substrate and in electrical contact with the plurality of lower source/drain regions of respective vertical MOS transistors.

3. The method of claim 1, further comprising:

depositing a second auxiliary layer, capable of wafer bonding, on the first auxiliary carrier substrate;

attaching a second auxiliary carrier substrate to the second auxiliary layer;

removing the first auxiliary carrier substrate and the first auxiliary layer;

forming metal bit lines on the second auxiliary carrier substrate for making direct electrical contact with the plurality of upper source/drain regions.

4. The method of claim 1, wherein the substrate and ribs are components of an SOI substrate comprising a buried oxide layer and further comprising removing the buried oxide layer prior to forming the plurality of lower source/drain regions on the ribs.

5. The method of claim 1, wherein forming the plurality of upper and lower source/drain regions comprises implanting doping ions.

6. The method of claim 1, wherein etching the trenches is done using lithographically produced mask patterns.

7. A DRAM cell arrangement with vertical MOS transistors, comprising:

a matrix of memory cells defined by a plurality of spaced-apart parallel word lines and a plurality of spaced-apart parallel ribs disposed in a cross-wise direction with respect to the word lines, wherein a memory cell is defined at each cross point defined by an intersection of a word line and a rib, wherein each memory cell comprises a vertical dual-gate MOS transistor each comprising:

an upper source/drain region, a lower source/drain region and a channel region disposed between the source/drain regions; wherein the channel region is formed in one of the ribs; and

a pair of gate electrodes formed on opposite sides of the channel region.

8. The DRAM cell arrangement of claim 7, wherein the upper source/drain regions are formed in strips of material traversing the lengths of the ribs.

9. The DRAM cell arrangement of claim 7, further comprising spaced-apart shallow isolation trenches disposed parallel to the word lines and formed on the ribs to isolate the lower source/drain regions from one another.

10. The DRAM cell arrangement of claim 7, further comprising trenches formed between the ribs and integrally connected with the word lines.

11. The DRAM cell arrangement of claim 7, wherein a width and doping of the channel regions is selected to produce fully depleted vertical dual-gate MOS transistors.

12. The DRAM cell arrangement of claim 7, wherein the gate electrodes formed by a gate dielectric layer disposed over the ribs.

13. The DRAM cell arrangement of claim 12, wherein a portion of the gate dielectric layer is disposed between the ribs and word lines.

14. The DRAM cell arrangement of claim 7, wherein each memory cell further comprises a capacitor electrically connected to a respective transistor

15. The DRAM cell arrangement of claim 14, wherein each capacitor is stacked with respect to its respective transistor and is electrically connected to the lower source/drain region of its respective transistor.

16. The DRAM cell arrangement of claim 15, further comprising metal bit lines disposed over the transistors and arranged parallel to the ribs and cross-wise with respect to the word lines, the metal bit lines being electrically connected to the upper source/drain regions of the respective transistors.

17. The DRAM cell arrangement of claim 15, further comprising an auxiliary carrier substrate disposed beneath the capacitors and an auxiliary layer capable of wafer bonding disposed between the auxiliary carrier substrate and the capacitors.

18. A DRAM cell arrangement with vertical MOS transistors, comprising:

a matrix of memory cells defined by the collective intersections of a plurality of spaced-apart parallel word lines and a plurality of spaced-apart parallel ribs disposed in a cross-wise direction with respect to the word lines, the ribs being covered with a gate dielectric material to form gate electrodes on each side of a respective rib and wherein the ribs are separated by trenches filled with conductive material in contact with the word lines, wherein each memory cell comprises a capacitor and a vertical dual-gate MOS transistor in stacked relation to one another and electrically connected, each vertical dual-gate MOS transistor comprising:

an upper source/drain region, a lower source/drain region and a channel region disposed between the source/drain regions; wherein the upper and lower source/drain regions are formed as strips of doped material traversing the lengths of their respective rib, and wherein the channel region is formed in one of the ribs and is grounded to at least reduce floating body effects.

19. The DRAM cell arrangement of claim 18, further comprising spaced-apart shallow isolation trenches disposed parallel to the word lines and formed on the ribs to isolate the lower source/drain regions from one another.

20. The DRAM cell arrangement of claim 18, wherein a width and doping of the channel regions is selected to produce fully depleted vertical dual-gate MOS transistors.

21. The DRAM cell arrangement of claim 18, wherein a portion of the gate dielectric layer is disposed between the ribs and word lines.

22. The DRAM cell arrangement of claim 18, wherein each capacitor is electrically connected to the lower source/drain region of its respective transistor.

23. The DRAM cell arrangement of claim 22, further comprising metal bit lines disposed over the transistors and arranged parallel to the ribs and cross-wise with respect to the word lines, the metal bit lines being electrically connected to the upper source/drain regions of the respective transistors.

24. The DRAM cell arrangement of claim 22, further comprising an auxiliary carrier substrate disposed beneath the capacitors and an auxiliary layer capable of wafer bonding disposed between the auxiliary carrier substrate and the capacitors.